REMARKS

Claims 1-11 are pending in the application. Claims 1, 9, 10, and 11 have been amended, leaving claims 1-11 for consideration upon entry of the present Amendment. Support for the amendment can be found at page 11, line 14 to page 12, line 15.

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the submitted prior art in Figure 1. For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988).

Figure 1 does not disclose all of the limitations of the claims. Claims 1, 9, 10, and 11, as amended, include the following limitations: "said first thin film transistor is a double gate type having a lightly doped drain structure * * * said second thin film transistor has a p-channel." The prior art in Figure 1 does not show that the first thin film transistor is a lightly doped drain structure and that the second thin film transistor is a p-channel. In addition, Applicant respectfully submits that it is not well known in the art to have a double gate type thin film transistor having a lightly doped drain structure. By using a double gate thin film transistor as the first thin film transistor, a reduction in a leakage current is obtained. Also, by using a p-channel thin film transistor as the second thin film transistor, variation in the drain current caused by the drain voltage can be reduced. See the Specification at page16, lines 14-19 and page 17, lines 6-13.

The requirement for a determination of obviousness is that "both the suggestion and the expectation of success must be founded in the prior art, not in applicant's disclosure." *In re Dow Chem.*, 837 F.2d 469, 473, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) (emphasis added). An Examiner cannot base a determination of obviousness on what the skilled person in the art might try or find obvious to try. Rather, the proper test requires determining what the prior art would have led the skilled person to do, with a reasonable expectation of success. In this case, the suggestion to combine a double gate type thin film transistor with a lightly doped drain structure comes from Applicant's disclosure and not Figure 1.

Because the prior art in Figure 1 does not disclose, teach, or suggest all of the limitations of claims 1, 9, 10, and 11, claims 1, 9, 10, and 11 are not obvious over Figure 1. In addition, claims 2-8 include all of the limitations of claim 1, and thus, claims 2-8 are not obvious over Figure 1. Accordingly, Applicants respectfully request that this rejection be withdrawn.

Claims 1-6 and 8-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohtani (U.S. 6,277,679). Applicant submits herewith a certified translation of the

priority document, Japanese Patent Application No. 11-12280. The priority document was filed on January 20, 1999. Ohtani has a filing date of November 24, 1999. Because the priority document has an earlier filing date than Ohtani, Applicants have properly antedated Ohtani. Accordingly, Applicants respectfully request that this rejection be withdrawn.

In addition, attached hereto is a marked-up version of the changes made to the application. The attached page is captioned "**Version with Markings to Show Changes Made.**"

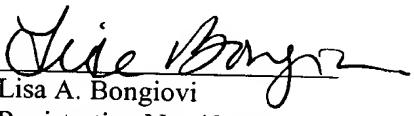
In view of the foregoing, it is respectfully submitted that the instant application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance issued. If the Examiner believes that a telephone conference with Applicant's attorneys would be advantageous to the disposition of this case, the Examiner is cordially requested to telephone the undersigned.

In the event the Commissioner of Patents and Trademarks deems additional fees to be due in connection with this application, Applicant's attorney hereby authorizes that such fee be charged to Deposit Account No. 06-1130.

Respectfully submitted,

TSUTOMU YAMADA

CANTOR COLBURN LLP
Applicant's Attorneys

By: 
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Version with Markings to Show Changes Made

IN THE CLAIMS:

Please amend claims 1, 9, 10, and 11 in "marked up" format, as follows:

1. (Marked up/Amended) An electroluminescence device, comprising:

an electroluminescence element having a light emissive layer provided between first and second electrodes;

a first thin film transistor receiving a selection signal at its gate to acquire a data signal; and

a second thin film transistor provided between a driving power supply and said electroluminescence element, and controlling power supplied from said driving power supply to said electroluminescence element in accordance with the data signal supplied from said first thin film transistor; wherein

said first thin film transistor is a double gate type having a lightly doped drain structure, said first thin film transistor has an n-channel, ~~and at least one of a lightly doped drain structure,~~ an offset structure, and a multigate structure; and

said second thin film transistor has a p-channel.

9. (Marked up/Amended) An electroluminescence display device, comprising:

an electroluminescence element having a light emissive layer provided between an anode and a cathode;

a first thin film transistor having an active layer which is formed of a non-single crystalline semiconductor film and which includes a source connected to a storage capacitor, a drain connected to a drain signal line, and a gate electrode provided over a channel of said active layer and connected to a gate signal line; and

a second thin film transistor having an active layer which is formed of a non-single crystalline semiconductor film and which includes a drain connected to a driving power supply of said electroluminescence element, and a gate electrode connected to the source of said first thin film transistor; wherein

said first thin film transistor is a double gate type having a lightly doped drain structure, said first thin film transistor has an n-channel ~~and at least one of a lightly doped drain structure~~, an offset structure, and a multigate structure; and

said second thin film transistor has a p-channel.

10. (Marked up/Amended) An electroluminescence display device, comprising:

an electroluminescence element having a light emissive layer provided between an anode and a cathode;

a first thin film transistor having an active layer which is formed of a non-single crystalline semiconductor film and which includes a source connected to a storage capacitor, a drain connected to a drain signal line, and a gate electrode provided under a channel of said active layer and connected to a gate signal line; and

a second thin film transistor having an active layer which is formed of a non-single crystalline semiconductor film and which includes a drain connected to a driving power supply of said electroluminescence element, and a gate electrode connected to the source of said first thin film transistor; wherein

said first thin film transistor is a double gate type having a lightly doped drain structure, said first thin film transistor has an n-channel ~~and at least one of a lightly doped drain structure~~, an offset structure, and a multigate structure; and

said second thin film transistor has a p-channel.

11. (Marked up/Amended) A light emissive device, comprising:

a light emissive element having a light emissive layer provided between first and second electrodes;

a first thin film transistor receiving a selection signal at its gate to acquire a data signal; and

a second thin film transistor provided between a driving power supply and said element, and controlling power supplied from said driving power supply to said element in accordance with the data signal supplied from said first thin film transistor; wherein

said first thin film transistor is a double gate type having a lightly doped drain structure, said first thin film transistor has an n-channel, ~~and at least one of a lightly doped drain structure,~~ an offset structure, and a multigate structure; and

said second thin film transistor has a p-channel.